REMARKS

Claims 3-6 are pending and under consideration. Claims 5 and 6 have been amended to overcome the 35 USC 112 rejection. Claims 3 and 4 have also been amended. The specification has been amended. Figs. 11M, 12, 14, 19 and 21 have been amended (attached replacement sheets). No new matter is presented.

Support for the amendments to claims 3 and 4 can be found in the specification. Namely, in the program mode and read mode, whose timing charts are shown in Figs. 9, 16 and Figs. 10, 17, respectively, seeing wave forms concerning WL0 and WL1 - WL16383, it is clear that both a select word line and non-select word lines are selected line-by-line, i.e. line-wise. While, in the erase mode, whose timing charts are shown in Figs. 11 and 18, seeing wave forms concerning WL0 - WL31 and WL32 - WL16383, it is clear that both the select word lines (Block 0: WL0 - WL31) and non-select word lines (Blocks 1 - 511: WL32 - WL16383) are selected block-by-block, i.e. block-wise.

The Examiner noted that Figs. 19 and 21 should be labeled prior art. These figures have been modified in accordance with the Examiner's suggestion.

The drawing were objected to as failing to comply with 37 CFR 1.84(p)(5) because they include reference signs not mentioned in the specification.

With regard to almost all of the reference signs mentioned by the Examiner, these reference signs are indeed mentioned in the description. Specifically, with regard to Fig. 3, the Examiner asserts that "hrdab, 0, hrdab and 31" are not shown. However, "hrdab" and "0" are intended to be one reference and are written in the manner shown because of space

considerations. Further, "hrdab 0" is disclosed in the specification at page 28, line 9. The same holds true for "hrdab 31". Further, it is obvious from the drawing and the specification that these reference symbols are intended to go together. Support for "hrdab 31" can be found at pg. 27, lines 9-11 (where i = 0 to 31).

Regarding Fig. 4, support for "erssetupb" can be found at pg. 31, line 9. Support for "hnset" can be found at pg. 31, line 10.

Regarding Fig. 5, "hhvpre" can be found at pg. 32, line 4, "hnvpnx" can be found at pg. 43, line 2, "hnvneg" can be found at page 32, line 5, "hnset" can be found at pg. 31, line 10, "n1" can be found at pg. 35, line 15, "n2" can be found at pg. 35, line 16, "P3" can be found at pg. 36, line 5, "P4" can be found at page 36, line 10, N7-N11 can be found at page 35, lines 8 and 14 and page 36, line 7.

Regarding Fig. 6, "erssetup" can be found at pg. 37, line 10, "sel0" can be found at page 31, line 2, "hners" can be found at pg. 37, line 15, "hnn0" can be found at pg. 37, line 15, "n3" can be found at pg. 37, line 14, "P5" can be found at pg. 37, line 11, "P6" can be found at pg. 48, line 3, "N13" can be found at pg. 48, line 4, and "N14" can be found at pg. 37, line 13.

Regarding Fig. 7, the NAND and NOR gates are not reference signs and thus do not need to be described in the specification. Further, 37 CFR 1.83(a) states that "conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation." As stated in the specification, at page 26, lines 16-24, the block decoder and the precoder are known technologies and their description

was intentionally omitted. This was completely proper under 37 CFR 1.83(a). The same can be said for Fig. 8.

Regarding Fig. 9, Applicant respectfully submits that each and every reference sign can be located in the specification. For instance, "hnvneg1" can be found at pg. 32, line 5, "xawlb" can be found at pg. 30, line 11, "nxwlb" can be found at pg. 30, line 14, and "hhvpre1" can be found at pg. 31, line 18. The same can be said for Figs. 10 and 11. Applicant submits that each and every reference sign in Figs. 10 and 11 can be found upon careful review of the specification.

Regarding Fig. 12, each instance of "PCONTROL" has been removed. It is noted that "voltage circuit 0" and "voltage circuit 31" are supported by the disclosure at pg. 53, line 16 through pg. 54, line 8. Further, "hdrab" can be found in the table at pg. 67. The remaining reference signs noted by the Examiner have been discussed above in connection with at least Fig. 3.

Regarding Fig. 13, "prgsetup" can be found at pg. 63, line 18, "hnset" can be found at pg. 63, line 19, "n5" can be found at pg. 59, line 2, "erssetupb" can be found at pg. 63, line 17, "N21" and "N23" can be found at pg. 69, line 2, "N22" can be found at pg. 69, line 5, and "N24" can be found at pg. 69, line 6. The remaining elements, such as the transistors noted by the Examiner, are not reference signs and do not need to be disclosed in the specification according to 37 CFR 1.83(a), as discussed above.

Regarding Fig. 14, this drawing has been modified to remove reference sign "P11" and "N26," since these are not actually described in the specification and are not necessary to understanding the invention. The remaining reference signs all have support in the specification.

For example, "wlon" can be found at pg. 53, line 14, "prgsetup" can be found at pg. 53, line 13, "hhvpp" can be found at pg. 55, line 15, "n6" can be found at pg. 58, line 9, "n7" can be found at pg. 58, line 13, "P12" can be found at pg. 58, line 12, and "N25" can be found at pg. 58, line 11.

Regarding Fig. 15, Applicant submits that each reference sign shown is described in the specification. For example, "hhvpre" can be found at pg. 38, line 2, "hnvnnx" can be found at pg. 53, line 14, "hnvneg" can be found at pg. 59, line 5, "hnset" can be found at pg. 62, line 19, "sel0" can be found at pg. 31, line 2, "Vss" can be found at pg. 30, line 13, "N27" can be found at pg. 70, 22, N28-N30 can be found at pg. 70, line 11, "n8" can be found at pg. 70, line 23, "n9" can be found at pg. 70, line 13, "P13" can be found at pg. 71, line 20, "N31" can be found at pg. 71, line 25, "N32" can be found at pg. 59, line 14, "P14" can be found at pg. 60, line 9, and "hners" can be found at pg. 47, line 23.

Regarding Figs. 16-18, all of these elements are listed in other figures and have been discussed above.

In light of the foregoing, Applicant respectfully requests that this objection be withdrawn.

The specification was objected to because it does not include a summary of the invention section. While Applicant does not believe that the statute states that this section "must" be included, the specification has been amended to include the heading "Summary of the Invention" in the appropriate place and respectfully request that this objection be withdrawn.

Claims 3-6 are rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

With regard to item a), Applicant respectfully submits that all of the references now shown in the drawings are supported by the specification.

With regard to item b), Applicant respectfully submits that Fig. 3 is a block diagram of a row decoder and Figs. 4-8 are circuit diagrams of various parts of the row decoder shown in Fig. 3. Fig. 4 is a circuit diagram of the control voltage circuit, Fig. 5 is a circuit diagram of the select voltage circuit and Fig. 6 is a diagram of the non-select voltage circuit. In Fig. 4, for example, the p-channel transistors are labeled with a "P" followed by a number, for the purpose of distinguishing each transistor from another. The n-channel transistors are labeled in a similar fashion. At page 34, line 15, the specification describes that transistor P1 is a p-channel MOS transistor. The same description of the other transistors can likewise be found with a careful examination of the specification. Therefore, since the p-channel and n-channel transistors are clearly described in the specification, Applicant requests that this rejection be withdrawn.

With regard to item c), the Examiner does not understand how the second voltage applied to the non-select row lines has an absolute voltage not larger than an absolute value of the first negative voltage applied to the substrate during the erasing operation because the specification and drawings only disclose the situation in which these values are equal. However, Applicant submits that failing to provide a table in which exact values are set forth is unnecessary to provide one of ordinary skill in the art sufficient information to make and use the invention. One of ordinary skill in the art would clearly understand how to set these voltages in the manner described. Applicant suggests that undue experimentation would not be necessary to apply voltages where the absolute value of the non-select voltage is not larger than the absolute value of the negative voltage. The Examiner has failed to assert that **undue** experimentation would be necessary. The specification is not required to teach every detail of the invention, the specification need only explain how to make and use the invention without requiring an

inordinate amount of experimentation. Further, even if some experimentation were necessary to make and use the invention, this is permissible as long as this experimentation is not undue. In the case of this application, one would only need to substitute voltage values different than the -8 volts disclosed in the examples in the specification to make and use the claimed device. This would not be undue experimentation. The Examiner has not asserted that this would involve undue experimentation either. Therefore, Applicant respectfully asserts that the Examiner has failed to fulfill his burden of proving that the specification is not enabling and this rejection should be withdrawn.

With respect to item c), the Examiner states that he does not understand how the negative voltage, which is applied to the substrate or well, is generated. The abstract states that a voltage Vneg is applied to the substrate. Vneg is generally generated by a charge pump-type booster circuit that is used for flash memories. Applicant respectfully submits that the method of generating Vneg is well known in the art, as is apparent from the fact that a negative voltage is used in the prior art described in the present application (see, i.e., Table 1).

With respect to item d), the Examiner states that the feature of the absolute value of the select voltage is equal to the absolute value of the negative voltage applied to the substrate (as recited in claims 5 and 6) is not described in the specification or seen in the drawings. Claims 5 and 6 have been amended to recite that the absolute value of the **non-select** voltage is equal to the absolute value of the negative voltage applied to the substrate.

In light of the foregoing, Applicant respectfully requests that this rejection be withdrawn.

Claims 5 and 6 are rejected under 35 USC 112, second paragraph. Claims 5 and 6 have been amended to correct the lack of antecedent basis. Applicant respectfully requests that this rejection be withdrawn.

Claims 3-6 are rejected under 35 USC 102(b) as being anticipated by Yamamoto (U.S. Patent No. 5,959,890). This rejection is respectfully traversed.

First, Applicant notes that Yamamoto is not a valid 35 USC 102(b) reference because it issued less than one year before the filing of this application. Nevertheless, Applicant provides the following remarks.

The row selection circuit of Yamamoto applies a voltage of -8 V to unselected world lines in the special test mode, which is neither the ordinary reading mode nor the erase mode, but a type of program mode (see col. 5, line 55, through col. 6, line 5). Thereby, even if there is a memory cell whose threshold voltage reaches a minus level due to over-programming (over-writing) among memory cells, the memory cells can be evaluated. Yamamoto does not discuss the erase mode until col. 11, line 15, and the next paragraph discloses that voltages of -8 V, 10 V and -8 V are applied to the well, word line and source line, respectively, in the erase mode. This method of voltage application is the same as those of the prior art shown in Table 1 of the present specification in case of erasing and represents only an ordinary way in the art of flash memory. Yamamoto does not teach or suggest that the select voltage or non-select voltage is selected according to the control voltage during erase mode, as claimed in claim 3. Differing quite from this, the claimed invention selects or does not select word lines block-wise, i.e. block-by-block, as shown in Table 2 in case of erase (see: Select, WL0 -WL31, Vpp (10V); Non-select,

WL32 - WL16383, Vneg (-8V)) and applies a negative voltage of -8 V to non-selected word lines.

The essential difference between Yamamoto and the device of claim 3 is that Yamamoto relates to a special test mode as one of a program mode and refers only in this program mode to non-select word lines. Yamamoto is silent with respect to the claimed blocks (see claims 3 and 4). Yamamoto only discloses memory blocks (shown in Fig. 9). However, these memory blocks are not the same as the claimed plurality of blocks.

Further, Yamamoto discloses that each word line driver (shown in Fig. 4) drives a corresponding word line WL1, WL2, ...WL63, i.e. line-by-line, and does not drive word lines block-by-block, as claimed in claims 3 and 4. Thus, Yamamoto fails to teach or suggest applying, in an erase mode, select and non-select voltages to word lines block-by-block. Thus,

Claim 3 recites outputting a control voltage responsive to the select/non-select information, outputting a select voltage responsive to a select state, outputting a non-select voltage responsive to a non-select state, and then selecting (in the erase mode) either the select voltage or the non-select voltage according to the control voltage. The select voltage is output to the select word lines and the non-select voltage is output to the non-select word lines.

In addition, the Examiner asserts that the gate selection signals SG correspond to the claimed applied voltage selection means. Applicant respectfully disagrees. Yamamoto discloses that the row decoder 510 generates a plurality of gate selection signals SG_0, SG_1, SG_2, . . . in which any signal in response to the address signal ADD_i is turned to a high level which indicates the selection (col. 7, lines 20-24). However, Yamamoto does not state that the either the select voltage or the non-select voltage are selected based on the control voltage, as claimed. The

Examiner asserts that the control voltage corresponds to the signal DS_0. However, Yamamoto does not disclose that the gate selection signals are generated based on the signal DS_0. Further, although Yamamoto discloses an erase mode, the reference does not disclose that during this erase mode, the select voltage or non-select voltage are chosen according to the control voltage. In fact, the discussion of the erase mode in Yamamoto does not begin until column 11, line 15, as stated previously. Likewise, with respect to claim 4, Yamamoto does not teach or suggest choosing between a high voltage and a low voltage based on the control voltage. Thus, Yamamoto fails to teach or suggest the features of claims 3 and 4. Claims 5 and 6 are allowable at least due to their respective dependencies. Applicant respectfully requests that this rejection be withdrawn.

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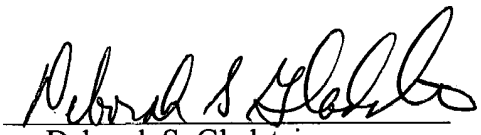
Dated: September 8, 2003

Respectfully submitted,

By: 

Deborah S. Gladstein
Registration No. 43,636

Morrison & Foerster LLP
1650 Tysons Boulevard
Suite 300
Mclean, VA 22102
Telephone: (703) 760-7753
Facsimile: (703) 760-7777